

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-305376
(43)Date of publication of application : 28.11.1997

(51)Int.Cl. G06F 5/06

B41J 2/01

G06F 3/12

G06F 12/02

(21) Application number : 08-149969

(71)Applicant : **BROTHER IND LTD**

(22) Date of filing : **20.05.1996**

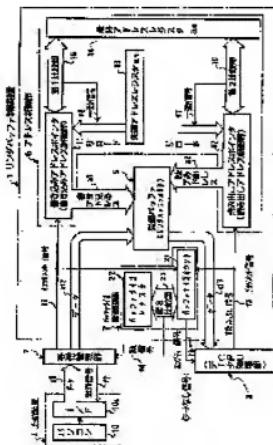
(72)Inventor : **HORI MASAAKI**

(54) RING BUFFER CONTROLLER AND IMAGE PRINTER USING SAME CONTROLLER

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a ring buffer controller which can facilitate the processing of a data processing part such as the image printer by being combined with the data processing part.

SOLUTION: Writing to a receiving buffer (ring buffer memory) 5 which received data d1 from a host device 4 and reading from this memory 5 are performed by hardware logic. This hardware logic gradually increases the address of writing to the memory 5 by a write address control part 11 and gradually decreases the address of reading from the memory 5 by a read address control part 12. When the write address or read address matches the tail address of the memory 5, the head address is reloaded to the write address control part 11 or read address control part 12 and the receiving buffer is used as the ring buffer memory. Further, a buffer size counter 21 is increased or decreased as each address gradually increase or decrease; when the receiving buffer 5 is full, a reception management part 2 outputs a busy signal and when the receiving buffer 5 is empty, a signal is processed part (CPU) 3.



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CLAIMS

[Claim(s)]

[Claim 1] When it has the following and said writing address and said final address are in agreement in said 1st comparing element, In [reload a start address of said head address register in said writing address control section, and] said 2nd comparing element, A ring-buffer-control device characterized by reloading a start address of said head address register in said read address controlling section when said reading address and said start address are in agreement. Writing to a ring buffer memory of data received from an upper device, And read-out from the memory is performed by hardware logic, By a data processing part, are the read data a ring-buffer-control device to process, and said hardware logic, A writing address control section which increases gradually a writing address to said ring buffer memory one by one based on an increment signal from a reception control department which receives data from said upper device.

A read address controlling section which dwindles a reading address from said ring buffer memory based on a decrement signal from said data processing part.

A head address register which stores a start address of said ring buffer memory.

The 1st comparing element that compares said writing address and said final address with the last address register which stores a final address of said ring buffer memory, and the 2nd comparing element that compares said reading address with said final address.

[Claim 2] When it has the following and enumerated data of said buffer size counter are in agreement with buffer size of said buffer size register with gradual increase of said writing address, Claim 1, wherein said 3rd comparing element outputs a coincidence signal to said reception control department in order to make a busy signal output to said upper device from said reception control department.

A buffer size register in which said hardware logic stores buffer size of said ring buffer memory further.

A buffer size counter which calculates size of a storing region of said ring buffer memory in response to said increment signal and a decrement signal.

The 3rd comparing element that compares buffer size of said buffer size register with enumerated data of said buffer size counter.

[Claim 3] A ring-buffer-control device characterized by outputting a data-less signal to said data processing part when said buffer size can uta shows that there is no stored data in said ring buffer memory in claim 2.

[Claim 4] An image printer, wherein it has one ring-buffer-control device of claims 1-3 and said data processing part is provided with a printing means which prints data.

[Claim 5] An image printer characterized by said printing means being the ink jet type print head which turns an ink droplet to print media and is spouted in claim 4.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] In this invention, it uses especially combining this ring-buffer-control device about the image printers (ink jet type recorder etc.) which use a ring-buffer-control device and the device.

Therefore, it is related with what can simplify composition of a data processing part.

[0002]

[Description of the Prior Art] Conventionally, in the image printer, data processing sent from a higher rank model was performed by the software logic by CPU based on the program included in the image printer.

[0003] For example, as shown in drawing 5, the image printer 102 is provided with CPU106, ROM108, RAM110, the navigational panel 112, the data input/output part 114, the print station interface 116, the print station part 118, the system bath 120, etc.

[0004] CPU106 is faced receiving data from the host computer 104 to a receive buffer via the data input/output part 114, or reading data from a receive buffer after that. When each address pointer of writing and read-out is increased gradually or dwindled, and a buffer size counter is fluctuated and a receive buffer fills, it controls to the host computer 104 for outputting a busy signal. Furthermore, CPU106 distinguishes the data read from the receive buffer, and when the data is character coded data, character pattern data are created, Bit map format data is created to the printing buffer in RAM110, and the print station part 118 must be controlled via the print station interface 116, and it must print on a print sheet.

[0005] By the way, since the demand of quality printing is increasing in recent years, the resolution of an image printer is becoming high gradually. High resolution and the metaphor must receive a maximum of 43,200 bytes of data by a party (it may be 60 dots by 8 inches) by the image printer of 720dpi as dot resolution.

[0006] When such a lot of printing data is stored in a storage area and it processes it, a printing area is used as a delay line memory, and the image printer of the ring-buffer-control method which raises the utilization ratio of a memory is proposed. Although an image printer prints this party for a short time, usually, In order to make it print with the maximum press speed of a printer, in addition to reception of data, said CPU106 needs to carry out ring buffer control, creation of print data, and processing required for printing and other control management from the host computer 104 as mentioned above between this short time. Usually, since CPU106 uses considerable time on reception of data among this short time, the time used for various control decreases. Since CPU106 also measures the active and inactive switching timing of a busy signal to the host computer 104 and it is performed, the time which can be used for the various control including ring buffer control decreases further.

[0007]

[Problem(s) to be Solved by the Invention] Thus, even if it adopts ring buffer control, the more

the resolution of an image printer, etc. improve, the more a lot of data expansion for a short time and its processing must be performed. Therefore, in order to make it print without reducing the press speed of an image printer, there was a problem that CPU106 [very high-speed] had to be used. Such a problem is produced in the general control device which develops not only an image printer but data by ring buffer control to the buffer in RAM108, and it controls by CPU106.

[0008]Then, an object of this invention is to provide the image printer using the ring-buffer-control device and the device which can simplify processing by a data processing part combining data processing parts, such as an image printer.

[0009]

[Means for Solving the Problem]In order to attain the purpose mentioned above, among this inventions an invention of claim 1, Writing to a ring buffer memory of data received from an upper device, And read-out from the memory is performed by hardware logic, By a data processing part, are the read data a ring-buffer-control device to process, and said hardware logic, A writing address control section which increases gradually a writing address to said ring buffer memory one by one based on an increment signal from a reception control department which receives data from said upper device, A read address controlling section which dwindles a reading address from said ring buffer memory based on a decrement signal from said data processing part, A head address register which stores a start address of said ring buffer memory, The last address register which stores a final address of said ring buffer memory, When it has the 1st comparing element that compares said writing address with said final address, and the 2nd comparing element that compares said reading address with said final address and said writing address and said final address are in agreement in said 1st comparing element, In [reload a start address of said head address register in said writing address control section, and] said 2nd comparing element, When said reading address and said start address are in agreement, a start address of said head address register is reloaded in said read address controlling section.

[0010]A writing address control section which increases a writing address gradually one by one, and a read address controlling section which dwindles a reading address, A head address register, the last address register, and the 1st comparing element that compares said writing address with said final address, An address control circuit which has the 2nd comparing element that compares said writing address with said final address is provided, and let a receive buffer be a ring buffer memory.

[0011]In claim 1, the invention according to claim 2 said hardware logic, A buffer size register which stores buffer size of said ring buffer memory, A buffer size counter which calculates size of a storing region of said ring buffer memory in response to said increment signal and a decrement signal, It has the 3rd comparing element that compares buffer size of said buffer size register with enumerated data of said buffer size counter, When enumerated data of said buffer size counter are in agreement with buffer size of said buffer size register with gradual increase of said writing address, said 3rd comparing element, In order to make a busy signal output to said upper device from said reception control department, a coincidence signal is outputted to said reception control department.

[0012]When an opening of a memory area is counted and an opening is lost by a buffer size control circuit provided with a buffer size register, a buffer size counter, and the 3rd comparing element, a busy signal is outputted to said upper device, and writing is made to halt.

[0013]When it is shown that, as for the invention according to claim 3, said buffer size can uta does not have stored data in said ring buffer memory in claim 2, a data-less signal is outputted to

said data processing part. The data processing part can know that there is no data in a ring buffer memory by this data-less signal.

[0014]It is an image printer, wherein the invention according to claim 4 is provided with one ring-buffer-control device of claims 1-3 and said data processing part is provided with a printing means which prints data. Since an image printer processes a lot of printing data, it can use this kind of ring-buffer-control device.

[0015]The invention according to claim 5 is an image printer, wherein said printing means is the ink jet type print head which turns an ink droplet to print media and is spouted in claim 4. High resolution is required and the amount of printing data of an image printer which has especially the ink jet type print head increases.

[0016]

[Embodiment of the Invention]An embodiment of the invention is described with the example of a graphic display. Drawing 1 is a block diagram of the ring-buffer-control device which is one embodiment of this invention.

[0017]In Drawing 1, it is connected between the reception control department 2 and CPU(data processing part) 3, and the ring-buffer-control device 1 is used. The reception control department 2 is connected to the upper device 4. The upper device 4 consists of the personal computer 10 and its interface 10a. The reception control department 2 receives the data d1 from the upper device 4, and transmits the busy signal f1 if needed to the upper device 4.

[0018]The ring-buffer-control device 1 which comprises hardware logic is provided with the following.

Receive buffer (ring buffer memory) 5.

Address control circuit 6.

Buffer size control circuit 7.

In order to use the receive buffer 5 as a ring buffer memory, while making a writing address increase gradually one by one, the address control circuit 6 dwindles a reading address, and specifies the writing position to the receive buffer 5, and a reading position. The buffer size control circuit 7 manages the residue of the memory area of the receive buffer 5.

[0019]The reception control department 2 outputs the data d2 to the receive buffer 5 while outputting the increment signal f2 to the address control circuit 6. And the address control circuit 6 specifies the predetermined address a1 with which said data d2 is written in to the receive buffer 5. This writing address a1 is increased gradually one by one. CPU(data processing part) 3 reads the data d3 from the receive buffer 5 while outputting the decrement signal f3 to the address control circuit 6. And the address control circuit 6 specifies the predetermined address a2 with which said data d3 is read to the receive buffer 5. This reading address a2 is dwindled one by one.

[0020]Below, the detailed composition of the address control circuit 6 as which the receive buffer 5 is operated as a ring buffer memory is explained. The address control circuit 6 is provided with the following.

Write address pointer (writing address control section) 11.

Read address pointer (read address controlling section) 12.

Head address register 13.

The last address register 14, the 1st comparing element 15, and the 2nd comparing element 16.

[0021]The write address pointer 11 increases gradually the writing address a1 to the receive buffer 5 one by one based on the increment signal f2 from the reception control department 2.

The read address pointer 12 dwindle the reading address a2 from the receive buffer 5 based on the decrement signal f3 from CPU3. The head address register 13 stores start-address a_f of the receive buffer 5, and the last address register 14 stores final address a_e of the receive buffer 5. [0022]When the 1st comparing element 15 compares the writing address a1 with final address a_e stored in the last address register 14 and the writing address a1 and final address a_e are in agreement, the coincidence signal f6 is outputted, Start-address a_f is reloaded in the write address pointer 11. That is, if it writes in to final address a_e of the address of the receive buffer 5, circulation of beginning writing from start-address a_f of the address of the receive buffer 5 will be performed.

[0023]The 2nd comparing element 16 compares the reading address a2 with final address a_e , when the reading address a2 and start-address a_f are in agreement, it outputs the coincidence signal f7, and it reloads start-address a_f of the head address register 13 in the read address pointer 12. That is, if it reads to final address a_e of the address of the receive buffer 5, circulation of beginning read-out from start-address a_f of the address of the receive buffer 5 will be performed.

[0024]As explained above, the address control circuit 6 is performing circulation control which reads data so that the writing of the data in the receive buffer 5 may be pursued, and it functions as using the memory area of the receive buffer 5 effectively. However, since it is necessary to manage the remaining memory areas in order to make possible the cyclic use of waste water of a memory area, the buffer size control circuit 7 is formed.

[0025]The buffer size control circuit 7 consists of the buffer size counter 21, the buffer size register 22, and the 3rd comparing element 23. The buffer size counter 21 calculates the size of the storing region of the receive buffer 5 (ring buffer memory) in response to the increment signal f2 and the decrement signal f3. The buffer size register 22 stores the buffer size which is the size of the storing region of the receive buffer 5. The 3rd comparing element 23 compares the enumerated data of the buffer size counter 21 with the buffer size of the buffer size register 22, When the enumerated data of the buffer size counter 21 are in agreement with the buffer size of the buffer size register 22, in order to make the busy signal f1 output to the upper device 4 from the reception control department 2, the coincidence signal f4 is outputted to the reception control department 2. The buffer size counter 21 will output the empty signal f5 to CPU(data processing part) 3, if data is completely lost to the storing region of the receive buffer 5, and CPU(data processing part) 3 enables it to perform required treatment.

[0026]It is based on the block diagram of drawing 1, and the flow chart figure of drawing 2 and drawing 3, and the operation of the ring-buffer-control device 1 which has next the hardware logic mentioned above is explained. Drawing 2 is flow chart figure showing the procedure of the data receiving processing by the ring-buffer-control device 1, and drawing 3 is a flow chart figure showing the procedure of the read signal processing by the ring-buffer-control device 1.

[0027]Drawing 1 and drawing 2 explain the procedure of data receiving processing first. The increment signal f2 and the received data d2 which are transmitted from the reception control department 2 based on the data d1 from the upper device 4 are received by the ring-buffer-control device 1 (S1). Especially the increment signal f2 is outputted to the write address pointer 11, as soon as it *****'s the writing address a1 (S2), is outputted also to the buffer size counter 21, and it *****'s the enumerated data (S11).

[0028]Based on the writing address a1 outputted from the write address pointer 11, the receive buffer 5 writes data in the position ordered with the writing address a1 from the write address pointer 11 (S3). With this writing, the writing address a1 from the write address pointer 11 is compared with last address register a_e by the 1st comparing element 15 (S4). If the coincidence

signal f6 is generated by the 1st comparing element 15 (S5, YES), start-address SHIJISUTA a_F will be reloaded in the write address pointer 11 (S6), and data receiving will be finished (S7). If the coincidence signal f6 is not generated by the 1st comparing element 15 (S5, NO), data receiving will be finished as it is (S7). By repeating the above flows S1-S7, data is received one after another.

[0029]On the other hand, after the increment signal f2 *****s the buffer size counter 21, the empty signal f5 is cleared (S12). And in the 3rd comparing element 23, enumerated data after *****ing the buffer size counter 21 are compared with the buffer size of the buffer size register 22 (S13). If the receive buffer 5 will be in a full state, the coincidence signal f4 is generated by the 3rd comparing element 23 (S14, YES), and the coincidence signal f4 is outputted to the reception control department 2, and the busy signal f1 will be generated in the reception control department 2, and it will be outputted to the upper device 4 (S15). If the coincidence signal f4 is not generated by the 3rd comparing element 23, a flow will be finished as it is (S16). The opening of the memory area of the receive buffer 5 is managed by repeating the flows S11-S16, whenever it receives an increment signal.

[0030]Drawing 1 and drawing 3 explain the procedure of data read processing below. It is outputted also to the buffer size counter 21 at the same time a read signal (decrement signal f3) is outputted to the read address pointer 12 from CPU(data processing part) 3 (S21). Based on this read signal (decrement signal f3), the data of the reading address a2 of the read address pointer 12 is transmitted to CPU3 (S22). Simultaneously, the decrement of the reading address a2 of the read address pointer 12 is carried out (S23). With this read-out, the reading address a2 in the read address pointer 12 is compared with last address register a_e by the 2nd comparing element 16 (S24). If the coincidence signal f7 is generated by the 2nd comparing element 16 (S25, YES), start-address SHIJISUTA a_F will be reloaded in the read address pointer 12 (S26), and data receiving will be finished (S27). If the coincidence signal f7 is not generated by the 2nd comparing element 16 (S25, NO), data receiving will be finished as it is (S27). By repeating the above flows S21-S27, data is read one after another.

[0031]On the other hand, the decrement signal f3 carries out the decrement of the buffer size counter 21 (S31). And in the 3rd comparing element 23, enumerated data after the decrement of the buffer size counter 21 was carried out are compared with the buffer size of the buffer size register 22 (S32). If read-out is carried out for the receive buffer 5 from a full state, the coincidence signal f4 is generated by the 3rd comparing element 23 (S33, YES), and the busy signal f1 from the reception control department 2 is canceled (S34), and if the receive buffer 5 is not full from the first. The coincidence signal f4 is not generated by the 3rd comparing element 23, but a flow is finished as it is (S35). The opening of the memory area of the receive buffer 5 is managed by repeating the flows S31-S35, whenever it receives a decrement signal.

[0032]It is judged whether enumerated data after the decrement of the buffer size counter 21 was carried out are zero (S36). The empty signal f5 is generated as it is zero, and it outputs to CPU3 (S37). (S36, YES) A flow will be finished if it is not zero (S36, NO) (S38).

[0033]Drawing 4 explains what is the image printer to which the ring-buffer-control device 1 mentioned above was applied, and has the ink jet type print head. In drawing 4, 9 is an image printer main part and 10 is a host computer.

[0034]The image printer main part 9 is provided with reception control department 2 and ring-buffer-control device 1, and CPU3. [which were mentioned above] The print station interface 35 is connected with ROM32, RAM33, and the navigational panel 34 at the system bath 31 to CPU3. The printhead actuator 36 for driving the ink jet type print head 38 for the print station

interface 35, The motor driving section 37 for driving CR motor 39 and the LF motor 40 for making a scanning direction and a vertical scanning direction carry out relative displacement of the record paper to the print head is connected.

[0035]Unlike the image printer of drawing 5, CPU3 transmits the decrement signal f3 to the gate array (the address control circuit 6 and the buffer size counter 7) in the ring-buffer-control device 1, and it reads the data d3 of an one pass from the receive buffer 5. It is as drawing 2 and drawing 3 having explained transfer of the data in the host computer 10, the reception control department 2, and the ring-buffer-control device 1. That is, CPU3 is released from the troublesome work of management of the address pointer of a receive buffer, or management of buffer size, and processing becomes easy. Therefore, CPU3 makes it possible to be able to concentrate on other functions required for printing, or to adopt cheap CPU3 which is not so high-speed, either.

[0036]The details of the ink jet type print head 38 are explained. The head 38, respectively For example, the recording head 38a for cyan ink in which 64 injection nozzles (recording element) were formed, respectively. The recording head 38b for magenta ink, the recording head 38c for yellow ink, and 38 d of recording heads for black ink are installed side by side and provided in the scanning direction. And to each of 64 injection nozzles (recording element) of each recording heads 38a-38b. When the piezoelectric element for ink jet is provided, respectively and 64 piezoelectric elements drive, with the color ink of four colors injected from two or more of these injection nozzles (recording element), it is full color in the record paper P, and image recording is carried out to it.

[0037]That is, it becomes possible to add various option functions or to manufacture the whole device cheaply, without the amount of data processing caring about restriction of the load of CPU about the image printer of full color printing which increases by leaps and bounds, if the ring-buffer-control device 1 mentioned above is applied.

[0038]

[Effect of the Invention]The writing to the ring buffer memory of data which the invention of claim 1 received from the upper device as explained above, And since it is the composition of performing read-out from the memory by hardware logic, and processing the read data by a data processing part, a data processing part, It is wide opened from the complicated control management for the writing to a ring buffer memory, and read-out, and while being able to concentrate on other processings, the effect which can use a cheap thing and to say is done so. Since hardware logic is a ring buffer method which circulates through and uses the data storing region of a memory, a memory area is used to the limit and the effect of raising the utilization ratio of a memory is done so.

[0039]The invention of claim 2 does so the effect of making possible much more unloading of a data processing part, raising the utilization ratio of a memory by controlling a reception control department so that in addition to the effect of raising the memory utilization ratio in claim 1 buffer size may be managed and a receive state may be controlled.

[0040]In addition to the effect of claims 1-2, hardware logic recognizes that data was lost to the memory area, and the invention of claim 3 sends a signal, and does so the effect of enabling data-less correspondence of said data processing part.

[0041]The invention of claim 4 does so especially the effect to what the effect of claims 1-3 equips with the printing means which prints data of being effective. While printing treats a lot of print data, finishing cheaply is because it asks.

[0042]The invention of claim 5 does so especially the effect of being effective, to the ink jet type

print head which the effect of claim 4 turns an ink droplet to print media, and spouts. The ink jet type print head is because high resolution is called for and processing of print data becomes complicated.

TECHNICAL FIELD

[Field of the Invention]In this invention, it uses especially combining this ring-buffer-control device about the image printers (ink jet type recorder etc.) which use a ring-buffer-control device and the device.

Therefore, it is related with what can simplify composition of a data processing part.

PRIOR ART

[Description of the Prior Art]Conventionally, in the image printer, data processing sent from a higher rank model was performed by the software logic by CPU based on the program included in the image printer.

[0003]For example, as shown in drawing 5, the image printer 102 is provided with CPU106, ROM108, RAM110, the navigational panel 112, the data input/output part 114, the print station interface 116, the print station part 118, the system bath 120, etc.

[0004]CPU106 is faced receiving data from the host computer 104 to a receive buffer via the data input/output part 114, or reading data from a receive buffer after that, When each address pointer of writing and read-out is increased gradually or dwindled, and a buffer size counter is fluctuated and a receive buffer fills, it controls to the host computer 104 for outputting a busy signal. Furthermore, CPU106 distinguishes the data read from the receive buffer, and when the data is character coded data, character pattern data are created, Bit map format data is created to the printing buffer in RAM110, and the print station part 118 must be controlled via the print station interface 116, and it must print on a print sheet.

[0005]By the way, since the demand of quality printing is increasing in recent years, the resolution of an image printer is becoming high gradually. High resolution and the metaphor must receive a maximum of 43,200 bytes of data by a party (it may be 60 dots by 8 inches) by the image printer of 720dpi as dot resolution.

[0006]When such a lot of printing data is stored in a storage area and it processes it, a printing area is used as a delay line memory, and the image printer of the ring-buffer-control method which raises the utilization ratio of a memory is proposed. Although an image printer prints this party for a short time, usually, In order to make it print with the maximum press speed of a printer, in addition to reception of data, said CPU106 needs to carry out ring buffer control, creation of print data, and processing required for printing and other control management from the host computer 104 as mentioned above between this short time. Usually, since CPU106 uses considerable time on reception of data among this short time, the time used for various control decreases. Since CPU106 also measures the active and inactive switching timing of a busy signal to the host computer 104 and it is performed, the time which can be used for the various control including ring buffer control decreases further.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, it is the composition of performing read-out from the writing and the memory to a ring buffer memory of the data received from the upper device by hardware logic in the invention of claim 1, and processing the read data by a data processing part.

Therefore, a data processing part is wide opened from the complicated control management for the writing to a ring buffer memory, and read-out, and it does so the effect which can use a cheap thing and to say while it can concentrate on other processings.

Since hardware logic is a ring buffer method which circulates through and uses the data storing region of a memory, a memory area is used to the limit and the effect of raising the utilization ratio of a memory is done so.

[0039] The invention of claim 2 does so the effect of making possible much more unloading of a data processing part, raising the utilization ratio of a memory by controlling a reception control department so that in addition to the effect of raising the memory utilization ratio in claim 1 buffer size may be managed and a receive state may be controlled.

[0040] In addition to the effect of claims 1-2, hardware logic recognizes that data was lost to the memory area, and the invention of claim 3 sends a signal, and does so the effect of enabling data-less correspondence of said data processing part.

[0041] The invention of claim 4 does so especially the effect to what the effect of claims 1-3 equips with the printing means which prints data of being effective. While printing treats a lot of print data, finishing cheaply is because it asks.

[0042] The invention of claim 5 does so especially the effect of being effective, to the ink jet type print head which the effect of claim 4 turns an ink droplet to print media, and spouts. The ink jet type print head is because high resolution is called for and processing of print data becomes complicated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Thus, even if it adopts ring buffer control, the more the resolution of an image printer, etc. improve, the more a lot of data expansion for a short time and its processing must be performed. Therefore, in order to make it print without reducing the press speed of an image printer, there was a problem that CPU106 [very high-speed] had to be used. Such a problem is produced in the general control device which develops not only an image printer but data by ring buffer control to the buffer in RAM108, and it controls by CPU106.

[0008] Then, an object of this invention is to provide the image printer using the ring-buffer-control device and the device which can simplify processing by a data processing part combining data processing parts, such as an image printer.

MEANS

[Means for Solving the Problem] In order to attain the purpose mentioned above, among this inventions an invention of claim 1, Writing to a ring buffer memory of data received from an upper device, And read-out from the memory is performed by hardware logic, By a data processing part, are the read data a ring-buffer-control device to process, and said hardware logic, A writing address control section which increases gradually a writing address to said ring buffer memory one by one based on an increment signal from a reception control department

which receives data from said upper device, A read address controlling section which dwindle a reading address from said ring buffer memory based on a decrement signal from said data processing part, A head address register which stores a start address of said ring buffer memory, The last address register which stores a final address of said ring buffer memory, When it has the 1st comparing element that compares said writing address with said final address, and the 2nd comparing element that compares said reading address with said final address and said writing address and said final address are in agreement in said 1st comparing element, In [reload a start address of said head address register in said writing address control section, and] said 2nd comparing element, When said reading address and said start address are in agreement, a start address of said head address register is reloaded in said read address controlling section.

[0010]A writing address control section which increases a writing address gradually one by one, and a read address controlling section which dwindle a reading address, A head address register, the last address register, and the 1st comparing element that compares said writing address with said final address, An address control circuit which has the 2nd comparing element that compares said writing address with said final address is provided, and let a receive buffer be a ring buffer memory.

[0011]In claim 1, the invention according to claim 2 said hardware logic, A buffer size register which stores buffer size of said ring buffer memory, A buffer size counter which calculates size of a storing region of said ring buffer memory in response to said increment signal and a decrement signal, It has the 3rd comparing element that compares buffer size of said buffer size register with enumerated data of said buffer size counter, When enumerated data of said buffer size counter are in agreement with buffer size of said buffer size register with gradual increase of said writing address, said 3rd comparing element, In order to make a busy signal output to said upper device from said reception control department, a coincidence signal is outputted to said reception control department.

[0012]When an opening of a memory area is counted and an opening is lost by a buffer size control circuit provided with a buffer size register, a buffer size counter, and the 3rd comparing element, a busy signal is outputted to said upper device, and writing is made to halt.

[0013]When it is shown that, as for the invention according to claim 3, said buffer size can uta does not have stored data in said ring buffer memory in claim 2, a data-less signal is outputted to said data processing part. The data processing part can know that there is no data in a ring buffer memory by this data-less signal.

[0014]It is an image printer, wherein the invention according to claim 4 is provided with one ring-buffer-control device of claims 1-3 and said data processing part is provided with a printing means which prints data. Since an image printer processes a lot of printing data, it can use this kind of ring-buffer-control device.

[0015]The invention according to claim 5 is an image printer, wherein said printing means is the ink jet type print head which turns an ink droplet to print media and is spouted in claim 4. High resolution is required and the amount of printing data of an image printer which has especially the ink jet type print head increases.

[0016]

[Embodiment of the Invention]An embodiment of the invention is described with the example of a graphic display. Drawing 1 is a block diagram of the ring-buffer-control device which is one embodiment of this invention.

[0017]In Drawing 1, it is connected between the reception control department 2 and CPU(data processing part) 3, and the ring-buffer-control device 1 is used. The reception control department

2 is connected to the upper device 4. The upper device 4 consists of the personal computer 10 and its interface 10a. The reception control department 2 receives the data d1 from the upper device 4, and transmits the busy signal f1 if needed to the upper device 4.

[0018]The ring-buffer-control device 1 which comprises hardware logic is provided with the following.

Receive buffer (ring buffer memory) 5.

Address control circuit 6.

Buffer size control circuit 7.

In order to use the receive buffer 5 as a ring buffer memory, while making a writing address increase gradually one by one, the address control circuit 6 dwindle a reading address, and specifies the writing position to the receive buffer 5, and a reading position. The buffer size control circuit 7 manages the residue of the memory area of the receive buffer 5.

[0019]The reception control department 2 outputs the data d2 to the receive buffer 5 while outputting the increment signal f2 to the address control circuit 6. And the address control circuit 6 specifies the predetermined address a1 with which said data d2 is written in to the receive buffer 5. This writing address a1 is increased gradually one by one. CPU(data processing part) 3 reads the data d3 from the receive buffer 5 while outputting the decrement signal f3 to the address control circuit 6. And the address control circuit 6 specifies the predetermined address a2 with which said data d3 is read to the receive buffer 5. This reading address a2 is dwindle one by one.

[0020]Below, the detailed composition of the address control circuit 6 as which the receive buffer 5 is operated as a ring buffer memory is explained. The address control circuit 6 is provided with the following.

Write address pointer (writing address control section) 11.

Read address pointer (read address controlling section) 12.

Head address register 13.

The last address register 14, the 1st comparing element 15, and the 2nd comparing element 16.

[0021]The write address pointer 11 increases gradually the writing address a1 to the receive buffer 5 one by one based on the increment signal f2 from the reception control department 2. The read address pointer 12 dwindle the reading address a2 from the receive buffer 5 based on the decrement signal f3 from CPU3. The head address register 13 stores start-address a_f of the receive buffer 5, and the last address register 14 stores final address a_e of the receive buffer 5.

[0022]When the 1st comparing element 15 compares the writing address a1 with final address a_e stored in the last address register 14 and the writing address a1 and final address a_e are in agreement, the coincidence signal f6 is outputted, Start-address a_f is reloaded in the write address pointer 11. That is, if it writes in to final address a_e of the address of the receive buffer 5, circulation of beginning writing from start-address a_f of the address of the receive buffer 5 will be performed.

[0023]The 2nd comparing element 16 compares the reading address a2 with final address a_e, when the reading address a2 and start-address a_f are in agreement, it outputs the coincidence signal f7, and it reloads start-address a_f of the head address register 13 in the read address pointer 12. That is, if it reads to final address a_e of the address of the receive buffer 5, circulation of beginning read-out from start-address a_f of the address of the receive buffer 5 will be performed.

[0024]As explained above, the address control circuit 6 is performing circulation control which reads data so that the writing of the data in the receive buffer 5 may be pursued, and it functions

as using the memory area of the receive buffer 5 effectively. However, since it is necessary to manage the remaining memory areas in order to make possible the cyclic use of waste water of a memory area, the buffer size control circuit 7 is formed.

[0025]The buffer size control circuit 7 consists of the buffer size counter 21, the buffer size register 22, and the 3rd comparing element 23. The buffer size counter 21 calculates the size of the storing region of the receive buffer 5 (ring buffer memory) in response to the increment signal f2 and the decrement signal f3. The buffer size register 22 stores the buffer size which is the size of the storing region of the receive buffer 5. The 3rd comparing element 23 compares the enumerated data of the buffer size counter 21 with the buffer size of the buffer size register 22. When the enumerated data of the buffer size counter 21 are in agreement with the buffer size of the buffer size register 22, in order to make the busy signal f1 output to the upper device 4 from the reception control department 2, the coincidence signal f4 is outputted to the reception control department 2. The buffer size counter 21 will output the empty signal f5 to CPU(data processing part) 3, if data is completely lost to the storing region of the receive buffer 5, and CPU(data processing part) 3 enables it to perform required treatment.

[0026]It is based on the block diagram of drawing 1, and the flow chart figure of drawing 2 and drawing 3, and the operation of the ring-buffer-control device 1 which has next the hardware logic mentioned above is explained. Drawing 2 is flow chart figure showing the procedure of the data receiving processing by the ring-buffer-control device 1, and drawing 3 is a flow chart figure showing the procedure of the read signal processing by the ring-buffer-control device 1.

[0027]Drawing 1 and drawing 2 explain the procedure of data receiving processing first. The increment signal f2 and the received data d2 which are transmitted from the reception control department 2 based on the data d1 from the upper device 4 are received by the ring-buffer-control device 1 (S1). Especially the increment signal f2 is outputted to the write address pointer 11, as soon as it *****'s the writing address a1 (S2), is outputted also to the buffer size counter 21, and it *****'s the enumerated data (S11).

[0028]Based on the writing address a1 outputted from the write address pointer 11, the receive buffer 5 writes data in the position ordered with the writing address a1 from the write address pointer 11 (S3). With this writing, the writing address a1 from the write address pointer 11 is compared with last address register ae by the 1st comparing element 15 (S4). If the coincidence signal f6 is generated by the 1st comparing element 15 (S5, YES), start-address SHIJISUTA af will be reloaded in the write address pointer 11 (S6), and data receiving will be finished (S7). If the coincidence signal f6 is not generated by the 1st comparing element 15 (S5, NO), data receiving will be finished as it is (S7). By repeating the above flows S1-S7, data is received one after another.

[0029]On the other hand, after the increment signal f2 *****'s the buffer size counter 21, the empty signal f5 is cleared (S12). And in the 3rd comparing element 23, enumerated data after *****'ing the buffer size counter 21 are compared with the buffer size of the buffer size register 22 (S13). If the receive buffer 5 will be in a full state, the coincidence signal f4 is generated by the 3rd comparing element 23 (S14, YES), and the coincidence signal f4 is outputted to the reception control department 2, and the busy signal f1 will be generated in the reception control department 2, and it will be outputted to the upper device 4 (S15). If the coincidence signal f4 is not generated by the 3rd comparing element 23, a flow will be finished as it is (S16). The opening of the memory area of the receive buffer 5 is managed by repeating the flows S11-S16, whenever it receives an increment signal.

[0030]Drawing 1 and drawing 3 explain the procedure of data read processing below. It is

outputted also to the buffer size counter 21 at the same time a read signal (decrement signal f3) is outputted to the read address pointer 12 from CPU(data processing part) 3 (S21). Based on this read signal (decrement signal f3), the data of the reading address a2 of the read address pointer 12 is transmitted to CPU3 (S22). Simultaneously, the decrement of the reading address a2 of the read address pointer 12 is carried out (S23). With this read-out, the reading address a2 in the read address pointer 12 is compared with last address register a₀ by the 2nd comparing element 16 (S24). If the coincidence signal f7 is generated by the 2nd comparing element 16 (S25, YES), start-address SHIJISUTA a₁ will be reloaded in the read address pointer 12 (S26), and data receiving will be finished (S27). If the coincidence signal f7 is not generated by the 2nd comparing element 16 (S25, NO), data receiving will be finished as it is (S27). By repeating the above flows S21-S27, data is read one after another.

[0031]On the other hand, the decrement signal f3 carries out the decrement of the buffer size counter 21 (S31). And in the 3rd comparing element 23, enumerated data after the decrement of the buffer size counter 21 was carried out are compared with the buffer size of the buffer size register 22 (S32). If read-out is carried out for the receive buffer 5 from a full state, the coincidence signal f4 is generated by the 3rd comparing element 23 (S33, YES), and the busy signal f1 from the reception control department 2 is canceled (S34), and if the receive buffer 5 is not full from the first. The coincidence signal f4 is not generated by the 3rd comparing element 23, but a flow is finished as it is (S35). The opening of the memory area of the receive buffer 5 is managed by repeating the flows S31-S35, whenever it receives a decrement signal.

[0032]It is judged whether enumerated data after the decrement of the buffer size counter 21 was carried out are zero (S36). The empty signal f5 is generated as it is zero, and it outputs to CPU3 (S37). (S36, YES) A flow will be finished if it is not zero (S36, NO) (S38).

[0033]Drawing 4 explains what is the image printer to which the ring-buffer-control device 1 mentioned above was applied, and has the ink jet type print head. In drawing 4, 9 is an image printer main part and 10 is a host computer.

[0034]The image printer main part 9 is provided with reception control department 2 and ring-buffer-control device 1, and CPU3, [which were mentioned above] The print station interface 35 is connected with ROM32, RAM33, and the navigational panel 34 at the system bath 31 to CPU3. The printhead actuator 36 for driving the ink jet type print head 38 for the print station interface 35, The motor driving section 37 for driving CR motor 39 and the LF motor 40 for making a scanning direction and a vertical scanning direction carry out relative displacement of the record paper to the print head is connected.

[0035]Unlike the image printer of drawing 5, CPU3 transmits the decrement signal f3 to the gate array (the address control circuit 6 and the buffer size counter 7) in the ring-buffer-control device 1, and it reads the data d3 of an one pass from the receive buffer 5. It is as drawing 2 and drawing 3 having explained transfer of the data in the host computer 10, the reception control department 2, and the ring-buffer-control device 1. That is, CPU3 is released from the troublesome work of management of the address pointer of a receive buffer, or management of buffer size, and processing becomes easy. Therefore, CPU3 makes it possible to be able to concentrate on other functions required for printing, or to adopt cheap CPU3 which is not so high-speed, either.

[0036]The details of the ink jet type print head 38 are explained. The head 38, respectively For example, the recording head 38a for cyan ink in which 64 injection nozzles (recording element) were formed, respectively. The recording head 38b for magenta ink, the recording head 38c for yellow ink, and 38 d of recording heads for black ink are installed side by side and provided in

the scanning direction. And to each of 64 injection nozzles (recording element) of each recording heads 38a-38b. When the piezoelectric element for ink jet is provided, respectively and 64 piezoelectric elements drive, with the color ink of four colors injected from two or more of these injection nozzles (recording element), it is full color in the record paper P, and image recording is carried out to it.

[0037]That is, it becomes possible to add various option functions or to manufacture the whole device cheaply, without the amount of data processing caring about restriction of the load of CPU about the image printer of full color printing which increases by leaps and bounds, if the ring-buffer-control device 1 mentioned above is applied.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a block diagram of the ring-buffer-control device which is one embodiment of this invention.

[Drawing 2]It is a flow chart figure showing the procedure of the data receiving processing by the ring-buffer-control device of this invention.

[Drawing 3]It is a flow chart figure showing the procedure of the read signal processing by the ring-buffer-control device of this invention.

[Drawing 4]It is a block diagram of an image printer using the ring-buffer-control device of this invention.

[Drawing 5]It is a block diagram of the conventional image printer.

[Description of Notations]

- 1 Ring-buffer-control device
- 2 Reception control department
- 3 CPU (data processing part)
- 4 Upper device
- 5 receive buffer (ring buffer memory)
- 6 Address control circuit
- 7 Buffer size control circuit
- 11 write address pointer (writing address control section)
- 12 read address pointer (read address controlling section)
- 13 Head address register
- 14 The last address register
- 15 The 1st comparing element
- 16 The 2nd comparing element
- 21 Buffer size can uta
- 22 Buffer size register
- 23 The 3rd comparing element
- a1 writing address
- a2 reading address
- d1, d2, d3 data flow
- f1 busy signal
- f2 increment signal
- f3 Decrement signal

f4 Coincidence signal

f5 empty signal

[Translation done.]

特開平9-305376

(43)公開日 平成9年(1997)11月28日

(51)Int.Cl. ⁶	戴出記号	序内整理番号	F I	技術表示箇所
G 0 6 F 5/06			C 0 6 F 5/06	B
B 4 1 J 2/01			3/12	B
G 0 6 F 3/12			12/02	5 8 0 D
12/02	5 8 0		B 4 1 J 3/04	1 0 1 Z

審査請求 未請求 請求項の数5 FD (全10頁)

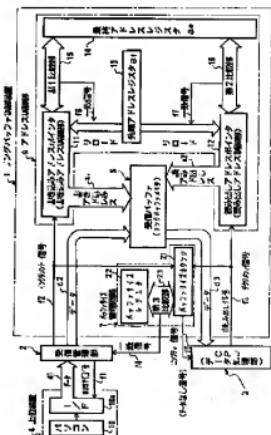
(21)出願番号	特願平8-149969	(71)出願人	000005267 ラザー工業株式会社 愛知県名古屋市瑞穂区苗代町15番1号
(22)出願日	平成8年(1996)5月20日	(72)発明者	堺 雅明 愛知県名古屋市瑞穂区苗代町15番1号 ブ ラザー工業株式会社内
		(74)代理人	弁理士 挿 良之

(54)【発明の名称】 リングバッファ制御装置および同装置を用いる画像印刷装置

(57)【要約】

【課題】 画像印刷装置等のデータ処理部と組み合わせて、データ処理部での処理を簡単にできることができるリングバッファ制御装置を提供する。

【解決手段】 上位装置4からデータd1を受信する受信バッファ(リングバッファメモリ)5への書き込み、および同メモリからの読み出しをハードウェアロジックにより実行する。そのハードウェアロジックは、書き込みアドレス制御部11によりメモリ5への書き込みアドレスを増し、読み出しアドレス制御部12によりメモリ5からの読み出しアドレスを削減する。書き込みアドレスまたは読み出しアドレスがメモリ5の最終アドレスに一致すると、先頭アドレスを書き込みアドレス制御部11または読み出しアドレス制御部12にリロードし、受信バッファをリングバッファメモリとして使用する。また、上記各アドレスの増減および削減に伴いバッファサイズカウンタ21を増減し、受信バッファ5が満杯の時、受信管理部2からビジー信号を出力させ、受信バッファ5が空の時、データ処理部(CPU)3にその旨の信号を出力する。



【特許請求の範囲】

【請求項1】 上位装置から受信したデータのリングバッファメモリへの書き込み、および同メモリからの読み出しをハードウェアロジックにより実行し、その読み出したデータをデータ処理部で処理するリングバッファ制御装置であって、

前記ハードウェアロジックは、

前記上位装置からデータを受信する受信管理部からのインクリメント信号に基づいて前記リングバッファメモリへの書き込みアドレスを順次漸増する書き込みアドレス制御部と、

前記データ処理部からのデクリメント信号に基づいて前記リングバッファメモリからの読み出しアドレスを漸減する読み出しアドレス制御部と、

前記リングバッファメモリの先頭アドレスを格納する先頭アドレスレジスタと、

前記リングバッファメモリの最終アドレスを格納する最終アドレスレジスタと、

前記書き込みアドレスと前記最終アドレスを比較する第1の比較部と、

前記読み出しアドレスと前記最終アドレスを比較する第2の比較部とを備え、

前記第1の比較部において、前記書き込みアドレスと前記最終アドレスが一致したとき、前記先頭アドレスレジスタの先頭アドレスを前記書き込みアドレス制御部にリロードし、

前記第2の比較部において、前記読み出しアドレスと前記先頭アドレスが一致したとき、前記先頭アドレスレジスタの先頭アドレスを前記読み出しアドレス制御部にリロードすることを特徴とするリングバッファ制御装置。

【請求項2】 請求項1において、前記ハードウェアロジックは、さらに、前記リングバッファメモリのバッファサイズを格納するバッファサイズレジスタと、前記インクリメント信号およびデクリメント信号を受けて前記リングバッファメモリの格納領域のサイズを計数するバッファサイズカウンタと、

前記バッファサイズレジスタのバッファサイズと前記バッファサイズカウンタの計数値を比較する第3の比較部とを備え、

前記書き込みアドレスの漸増にともない、前記バッファサイズカウンタの計数値が前記バッファサイズレジスタのバッファサイズと一致したとき、前記第3の比較部は、前記受信管理部から前記上位装置にビギ信号を出力させるために前記受信管理部に一致信号を出力することを特徴とするリングバッファ制御装置。

【請求項3】 請求項2において、前記バッファサイズカウンタが、前記リングバッファメモリでの格納データがないことを示したとき、前記データ処理部にデータ無し信号を出力することを特徴とするリングバッファ制御

装置。

【請求項4】 請求項1から3のいずれかのリングバッファ制御装置を備え、前記データ処理部は、データを印刷する印刷手段を備えることを特徴とする画像印刷装置。

【請求項5】 請求項4において、前記印刷手段は、インク滴を印刷媒体に向けて噴出するインクジェット式印刷ヘッドであることを特徴とする画像印刷装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は、リングバッファ制御装置において同装置を用いる画像印刷装置（インクジェット式記録装置等）に関し、特にこのリングバッファ制御装置と組み合わせて用いることによりデータ処理部の構成を簡単にできるものに関する。

【0002】

【従来の技術】 従来、画像印刷装置においては、上位機種から送られるデータ処理は、画像印刷装置に組み込まれたプログラムに基づくCPUによるソフトウェアロジックによって行われていた。

【0003】 例えば、図5に示すごとく、画像印刷装置102は、CPU106、ROM108、RAM110、操作パネル112、データ入出力部114、印刷機構インクフェース116、印刷機構部118およびシステムバス120などを備えている。

【0004】 CPU106はデータ入出力部114を介してホストコンピュータ104から受信バッファにデータを受信したり、その後受信バッファからデータを読み出すに際して、書き込み及び読み出しの各アドレスポイントを漸増または漸減し、またバッファサイズカウンタを増減し、受信バッファが溝杯になったとき、ホストコンピュータ104に対し、ビジー信号を出力するための制御をする。さらにCPU106は、受信バッファから読み出したデータを判別し、そのデータが文字コードデータであった場合には文字パターンデータを作成する等して、RAM110内の印刷バッファにビットマップ形式のデータを作成すると共に印刷機構インクフェース116を介して印刷機構部118を制御して、印刷用紙に印刷をしなければならない。

【0005】 ところで、近年、高品質の印刷の要求が高まっているため、画像印刷装置の解像度が次第に高くなっている。高解像度、例えば、ドット解像度として、720dp1の画像印刷装置では一行（縦60ドット×横8インチとする）で最大43,200バイトのデータを受信しなければならない。

【0006】 このような大量の印字データを記憶領域に格納して処理する場合に、印字領域を循環メモリとして使用し、メモリの使用効率を高めるリングバッファ制御方式の画像印刷装置が提案されている。普通、画像印刷装置は、この一行を短時間で印刷するが、プリンタの最

大の印刷速度で印刷を行わせるには、この短時間の間に、前記CPU106は、上記のようにホストコンピュータ104からデータの受信に加えて、リングバッファ制御、印刷データの作成、印刷に必要な処理やその他の制御処理を実施する必要がある。通常CPU106はこの短時間のうちデータの受信に相当の時間を使うので、各種制御に用いられる時間は少なくなる。また、ホストコンピュータ104に対するビジー信号のアクティブ・非アクティブの切替タイミングもCPU106が計測しておこなっているため、リングバッファ制御を含めた各種制御に使用できる時間は更に少なくなる。

【0007】

【発明が解決しようとする課題】このように、リングバッファ制御を採用したとしても、画像印刷装置の解像度などが向上すればするほど、より短時間に大量のデータ開票とその処理を行わなければならぬ。そのため、画像印刷装置の印刷速度を落とさずに印刷させるためには、亟めて高速のCPU106を使用しなければならないという問題点があった。なお、このような問題は、画像印刷装置に限らず、データをRAM108内のバッファにリングバッファ制御で開票し、CPU106で制御する制御装置一般において生じている。

【0008】そこで、本発明は、画像印刷装置等のデータ処理部と組み合わせて、データ処理部での処理を簡単にすることができるリングバッファ制御装置および開票装置を用いる画像印刷装置を提供することを目的としている。

【0009】

【課題を解決するための手段】前述した目的を達成するために、本発明のうちで請求項1の発明は、上位装置から受信したデータのリングバッファメモリへの書き込み、および同メモリからの読み出しをハードウェアロジックにより実行し、その読み出したデータをデータ処理部で処理するリングバッファ制御装置であって、前記ハードウェアロジックは、前記上位装置からデータを受信する受信管理部からのインクリメント信号に基づいて前記リングバッファメモリへの書き込みアドレスを順次増する書き込みアドレス制御部と、前記データ処理部からのデクリメント信号に基づいて前記リングバッファメモリからの読み出しアドレスを漸減する読み出しアドレス制御部と、前記リングバッファメモリの先頭アドレスを格納する先頭アドレスレジスタと、前記リングバッファメモリの最終アドレスを格納する最終アドレスレジスタと、前記書き込みアドレスと前記最終アドレスを比較する第1の比較部と、前記読み出しアドレスと前記最終アドレスを比較する第2の比較部とを備え、前記第1の比較部において、前記書き込みアドレスと前記最終アドレスが一致したとき、前記先頭アドレスレジスタの先頭アドレスを前記書き込みアドレス制御部にリロードし、前記第2の比較部において、前記読み出しアドレスと前記

記先頭アドレスが一致したとき、前記先頭アドレスレジスタの先頭アドレスを前記読み出しアドレス制御部にリロードすることを特徴とするものである。

【0010】書き込みアドレスを順次増する書き込みアドレス制御部と、読み出しアドレスを漸減させる読み出しアドレス制御部と、先頭アドレスレジスタと、最終アドレスレジスタと、前記書き込みアドレスと前記最終アドレスを比較する第1の比較部と、前記書き込みアドレスと前記最終アドレスを比較する第2の比較部とを有するアドレス制御回路を設けて、受信バッファをリングバッファメモリとしたものである。

【0011】また請求項2記載の発明は、請求項1において、前記ハードウェアロジックは、さらに、前記リングバッファメモリのバッファサイズを格納するバッファサイズレジスタと、前記リングバッファメモリのバッファサイズを計数するバッファサイズカウンタと、前記バッファサイズレジスタのバッファサイズと前記バッファサイズカウンタの計数値を比較する第3の比較部とを備え、前記書き込みアドレスの漸増とともに、前記バッファサイズカウンタの計数値と前記バッファサイズレジスタのバッファサイズと一致したとき、前記第3の比較部は、前記受信管理部から前記上位装置にビジー信号を出力させるために前記受信管理部に一致信号を出力することを特徴とするものである。

【0012】バッファサイズレジスタとバッファサイズカウンタと第3の比較部とを備えたバッファサイズ管理回路によって、メモリ領域の空きをカウントし、空きがなくなると前記上位装置にビジー信号を出力して書き込みを一時停止させる。

【0013】また請求項3記載の発明は、請求項2において、前記バッファサイズカウンタが、前記リングバッファメモリでの格納データがないことを示したとき、前記データ処理部にデータ無し信号を出力することを特徴とするものである。データ処理部によるデータ無し信号でリングバッファメモリにデータがないことを知ることが出来る。

【0014】また請求項4記載の発明は、請求項1から3のいずれかのリングバッファ制御装置を備え、前記データ処理部は、データを印刷する印刷手段を備えることを特徴とする画像印刷装置である。画像印刷装置は大量の印字データを処理するので、この種のリングバッファ制御装置が使用できる。

【0015】また請求項5記載の発明は、請求項4において、前記印刷手段は、インク滴を印刷媒体に向けて噴出するインクジェット式印刷ヘッドであることを特徴とする画像印刷装置である。特にインクジェット式印刷ヘッドを有する画像印刷装置は、高解像度が要求され、印字データ量が多くなる。

【0016】

【発明の実施の形態】本発明の実施の形態を、図示例とともに説明する。図1は本発明の一実施形態であるリングバッファ制御装置のブロック図である。

【0017】図1において、リングバッファ制御装置1は、受信管理部2とCPU(データ処理部)3との間に接続されて用いられる。また、受信管理部2は上位装置4に接続される。上位装置4は例えばパソコン10とそのインターフェース10aとからなっている。受信管理部2は上位装置4からデータd1を受信し、上位装置4に対して必要に応じてビギン信号f1を送信する。

【0018】ハードウェアロジックで構成されるリングバッファ制御装置1は、受信バッファ(リングバッファメモリ)5と、アドレス制御回路6と、バッファサイズ管理回路7とを備えてなる。受信バッファ5をリングバッファメモリとして使用するため、書き込みアドレスを順次漸増させるとともに、読み出しアドレスを漸減させて受信バッファ5に対する書き込み位置と読み出し位置を指定するのがアドレス制御回路6である。また受信バッファ5のメモリ領域の量を管理するのがバッファサイズ管理回路7である。

【0019】受信管理部2はインクリメント信号f2をアドレス制御回路6に出力するとともに、データd2を受信バッファ5に対して出力する。そして、アドレス制御回路6は前記データd2が書き込まれる所定のアドレスa1を受信バッファ5に対して指定する。この書き込みアドレスa1は順次漸増される。またCPU(データ処理部)3はデクリメント信号f3をアドレス制御回路6に出力するとともに、受信バッファ5からデータd3を読みだす。そして、アドレス制御回路6は前記データd3が読みだされる所定のアドレスa2を受信バッファ5に対して指定する。この読み出しアドレスa2は順次漸減される。

【0020】つぎに、受信バッファ5をリングバッファメモリとして機能させるアドレス制御回路6の詳細構成を説明する。アドレス制御回路6は、書き込みアドレスポインタ(書き込みアドレス制御部)11と、読み出しアドレスポインタ(読み出しアドレス制御部)12と、先頭アドレスレジスタ13と、最終アドレスレジスタ14と、第1比較部15と、第2比較部16とを備えてなる。

【0021】書き込みアドレスポインタ11は、受信管理部2からのインクリメント信号f2に基づいて受信バッファ5への書き込みアドレスa1を順次漸増する。読み出しアドレスポインタ12は、CPU3からのデクリメント信号f3に基づいて受信バッファ5からの読み出しアドレスa2を漸減させる。先頭アドレスレジスタ13は受信バッファ5の先頭アドレスa1を格納し、最終アドレスレジスタ14は受信バッファ5の最終アドレスa2を格納する。

【0022】第1の比較部15は、書き込みアドレスa

1と最終アドレスレジスタ14に格納された最終アドレスa。とを比較し、書き込みアドレスa1と最終アドレスa。が一致したとき一致信号f6を出力して、先頭アドレスa1を書き込みアドレスポインタ11にリロードする。すなわち、受信バッファ5のアドレスの最終アドレスa。まで書き込むと、受信バッファ5のアドレスの先頭アドレスa1から書き込みを始めるという循環を行う。

【0023】第2の比較部16は、読み出しアドレスa2と最終アドレスa。を比較し、読み出しアドレスa2と先頭アドレスa1が一致したとき一致信号f7を出力し、先頭アドレスレジスタ13の先頭アドレスa1を読み出しアドレスポインタ12にリロードする。すなわち、受信バッファ5のアドレスの最終アドレスa。まで読み込むと、受信バッファ5のアドレスの先頭アドレスa1から読み出しを始めるという循環を行う。

【0024】以上説明したように、アドレス制御回路6は、受信バッファ5におけるデータの書き込みを追いかけるようにデータの読み出しを行う循環制御を行っており、受信バッファ5のメモリ領域を効率的に使用するよう機能する。ただし、メモリ領域の循環使用を可能にするためには、残りのメモリ領域を管理する必要があるので、バッファサイズ管理回路7が設けられている。

【0025】バッファサイズ管理回路7は、バッファサイズカウンタ21と、バッファサイズレジスタ22と、第3比較部23とからなっている。バッファサイズカウンタ21は、インクリメント信号f2およびデクリメント信号f3を受けて受信バッファ5(リングバッファメモリ)の格納領域のサイズを計数する。バッファサイズレジスタ22は受信バッファ5の格納領域のサイズであるバッファサイズを格納する。第3の比較部23は、バッファサイズカウンタ21の計数値と、バッファサイズレジスタ22のバッファサイズとを比較し、バッファサイズカウンタ21が受信バッファ5の格納領域にデータが全くなくなると、CPU(データ処理部)3にエンブティ信号f5を出力し、CPU(データ処理部)3が必要な処理を実行できるようにする。

【0026】つぎに、上述したハードウェアロジックを有するリングバッファ制御装置1の動作を、図1のブロック図と、図2及び図3のフローチャート図に基づいて説明する。図2はリングバッファ制御装置1によるデータ受信処理の手順を示すフローチャート図であり、図3はリングバッファ制御装置1による読み出し信号処理の手順を示すフローチャート図である。

【0027】まずデータ受信処理の手順を図1及び図2により説明する。上位装置4からのデータd1にもとづ

いて受信管理部2から送信されるインクリメント信号f2と受信データd2がリングバッファ制御装置1で受信される(S1)。特にインクリメント信号f2は、書き込みアドレスポインタ11に出力され、書き込みアドレスa1をインクリメントする(S2)と同時に、バッファサイズカウンタ21にも出力され、その計数値をインクリメントする(S11)。

【0028】書き込みアドレスポインタ11から出力される書き込みアドレスa1に基づいて、受信バッファ5は書き込みアドレスポインタ11からの書き込みアドレスa1で指令された位置にデータを書き込む(S3)。この書き込みとともに、第1比較部15によって、書き込みアドレスポインタ11からの書き込みアドレスa1と最終アドレスレジスタa5が比較される(S4)。第1比較部15で一致信号f6が生成されると(S5, YES)、先頭アドレスシグナルafを書き込みアドレスポインタ11にリロードし(S6)、データ受信を終える(S7)。第1比較部15で一致信号f6が生成されないと(S5, NO)、そのままデータ受信を終える(S7)。以上のフローS1～S7を繰り返すことで、次々にデータが受信される。

【0029】一方、インクリメント信号f2がバッファサイズカウンタ21をインクリメントしたあと、エンブティ信号f5がクリアされる(S12)。そして、第3比較部23において、バッファサイズカウンタ21のインクリメントされたあととの計数値がバッファサイズレジスタ22のバッファサイズと比較される(S13)。受信バッファ5が満杯状態になると、第3比較部23で一致信号f4が生成され(S14, YES)、その一致信号f4が受信管理部2に出力され、受信管理部2でビジー信号f1が生成されて上位装置4に出力される(S15)。第3比較部23で一致信号f4が生成されないと、そのままフローを終える(S16)。インクリメント信号を受けるたびに、フローS11～S16を繰り返すことで、受信バッファ5のメモリ領域の空きを管理する。

【0030】つぎにデータ読み出し処理の手順を図1及び図3により説明する。CPU(データ処理部)3から読み出し信号(デクリメント信号f3)が読み出しアドレスポインタ12に出力されると同時に、バッファサイズカウンタ21にも出力される(S21)。この読み出し信号(デクリメント信号f3)に基づいて、読み出しアドレスポインタ12の読み出しアドレスa2のデータをCPU3に転送する(S22)。同時に、読み出しアドレスポインタ12の読み出しアドレスa2をデクリメントする(S23)。この読み出しとともに、第2比較部16によって、読み出しアドレスポインタ12での読み出しアドレスa2と最終アドレスレジスタa5が比較される(S24)。第2比較部16で一致信号f7が生成されると(S25, YES)、先頭アドレスシグ

タafを読み出しアドレスポインタ12にリロードし(S26)、データ受信を終える(S27)。第2比較部16で一致信号f7が生成されないと(S25, NO)、そのままデータ受信を終える(S27)。以上のフローS21～S27を繰り返すことで、次々にデータが読みだされる。

【0031】一方、デクリメント信号f3がバッファサイズカウンタ21をデクリメントする(S31)。そして、第3比較部23において、バッファサイズカウンタ21のデクリメントされたあととの計数値がバッファサイズレジスタ22のバッファサイズと比較される(S32)。受信バッファ5が満杯状態の読み出し сигナルが生成されると、第3比較部23で一致信号f4が生成され(S33, YES)、受信管理部2からのビジー信号f1が解除され(S34)、受信バッファ5がもともと満杯でなければ、第3比較部23で一致信号f4が生成されず、そのままフローを終える(S35)。デクリメント信号を受けるたびに、フローS31～S35を繰り返すことで、受信バッファ5のメモリ領域の空きを管理する。

【0032】またバッファサイズカウンタ21のデクリメントされたあととの計数値がゼロになっているかどうか判断する(S36)。ゼロであると(S36, YES)、エンブティ信号f5を生成し、CPU3に出力する(S37)。ゼロでないと(S36, NO)、フローを終える(S38)。

【0033】さらに、上述したリングバッファ制御装置1が適用された画像印刷装置であってインジェット式印刷ヘッドを有するものを図4により説明する。図4において、9は画像印刷装置本体であり、10はホストコンピュータである。

【0034】画像印刷装置本体9は、前述した受信管理部2とリングバッファ制御装置1とCPU3を備える。CPU3に対するシステムバス31には、ROM32と、RAM33と、操作パネル34と、印刷機構インターフェース35が接続されている。また、印刷機構インターフェース35には、インクジェット式印刷ヘッド38を駆動するための印字ヘッド駆動部36と、記録用紙を印刷ヘッドに対して主走査方向及び副走査方向に相対移動させるためのCRモータ39とLFモータ40を駆動するためのモータ駆動部37が接続されている。

【0035】図5の画像印刷装置と異なり、CPU3はリングバッファ制御装置1内のゲートアレイ(アドレス制御回路6)とバッファサイズカウンタ7)に対してデクリメント信号f3を送信して、受信バッファ5から1バク相当のデータ3を読みだす。なお、ホストコンピュータ10と受信管理部2及びリングバッファ制御装置1におけるデータの授受については図2及び図3で説明した通りである。すなわち、CPU3は受信バッファのアドレスポインタの管理やバッファサイズの管理という面

倒な作業から解放され、処理が簡単になる。したがって、CPU3が印刷に必要な他の機能に専念することができたり、それほど高速でもない安価なCPU3を採用することを可能にする。

【0036】さらに、インクジェット式印刷ヘッド38の詳細を説明する。ヘッド38は、それぞれ例えば64個の噴射ノズル（記録素子）がそれぞれ形成されたシアシンク用記録ヘッド38aと、マゼンダインク用記録ヘッド38bと、エイローアイント用記録ヘッド38cと、ブラックインク用記録ヘッド38dとが、主走査方向に並設して設けられている。そして、各記録ヘッド38a～38bの64個の噴射ノズル（記録素子）の各々には、インク噴射のための圧電素子がそれぞれ設けられ、64個の圧電素子が駆動されることにより、これらの複数の噴射ノズル（記録素子）から噴射された4色のカラーリングにより、記録用紙Pにフルカラーで画像記録される。

【0037】すなわち、前述したリングバッファ制御装置1を適用すると、データ処理量が飛躍的に増大するフルカラー印字の画像印刷装置について、CPUの負荷の制限を気にすることなく、種々のオプション機能を付加したり、装置全体を安価に製造することができるようになる。

【0038】

【発明の効果】以上説明したように、請求項1の発明は、上位装置から受信したデータのリングバッファメモリへの書き込み、および同メモリからの読み出しをハードウェアロジックにより実行し、その読み出したデータをデータ処理部で処理する構成であるので、データ処理部は、リングバッファメモリへの書き込みおよび読み出しのための複雑な制御処理から開放され、他の処理に専念できるとともに安価のものを使用できるという効果を奏する。また、ハードウェアロジックはメモリのデータ格納領域を循環して使用するリングバッファ方式であるので、メモリ領域を一杯に使用して、メモリの使用効率を高めるという効果を奏す。

【0039】請求項2の発明は、請求項1におけるメモリ使用効率を高めるという効果に加えて、バッファサイズを管理して受信状態を制御するように、受信管理部を制御することによって、メモリの使用効率を高めつつデータ処理部の一層の負荷軽減を可能にするという効果を奏する。

【0040】請求項3の発明は、請求項1から2の効果に加えて、メモリ領域にデータが無くなったことをハードウェアロジックが認識して信号を送り、前記データ処理部のデータ無し対応を可能にするという効果を奏する。

【0041】請求項4の発明は、請求項1から3の効果

が、データを印刷する印刷手段を備えるものに対してと、特に有効であるという効果を奏する。なぜならば、印刷は大量の印刷データを扱うとともに、安価に仕上げることが求められるからである。

【0042】請求項5の発明は、請求項4の効果が、インク滴を印刷媒体に向けて噴出するインクジェット式印刷ヘッドに対して特に有効であるという効果を奏する。なぜならば、インクジェット式印刷ヘッドは高い解像度が求められ、印刷データの処理が複雑になるからである。

【図面の簡単な説明】

【図1】本発明の一実施形態であるリングバッファ制御装置のブロック図である。

【図2】本発明のリングバッファ制御装置によるデータ受信処理の手順を示すフローチャート図である。

【図3】本発明のリングバッファ制御装置による読み出し信号処理の手順を示すフローチャート図である。

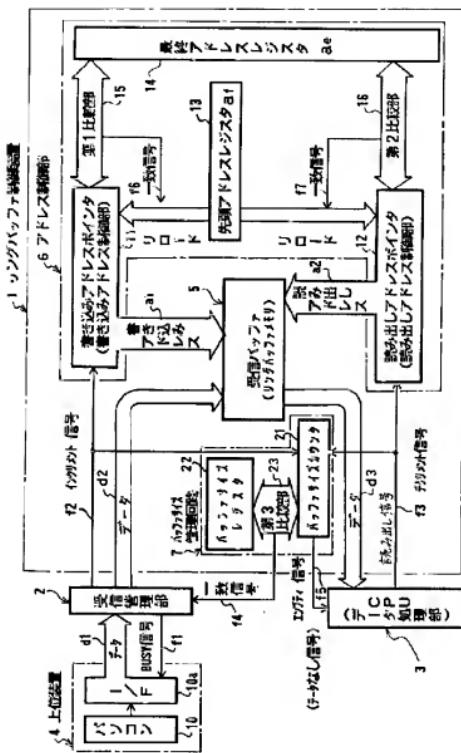
【図4】本発明のリングバッファ制御装置を用いた画像印刷装置のブロック図である。

【図5】従来の画像印刷装置のブロック図である。

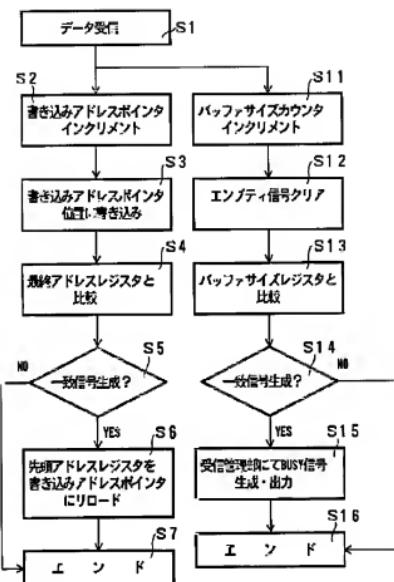
【符号の説明】

- 1 リングバッファ制御装置
- 2 受信管理部
- 3 CPU（データ処理部）
- 4 上位装置
- 5 受信バッファ（リングバッファメモリ）
- 6 アドレス制御回路
- 7 バッファサイズ管理回路
- 1.1 書き込みアドレスポイント（書き込みアドレス制御部）
- 1.2 読み出しアドレスポイント（読み出しアドレス制御部）
- 1.3 先頭アドレスレジスタ
- 1.4 最終アドレスレジスタ
- 1.5 第1比較部
- 1.6 第2比較部
- 2.1 バッファサイズカンウタ
- 2.2 バッファサイズレジスタ
- 2.3 第3比較部
- a.1 書き込みアドレス
- a.2 読み出しアドレス
- d.1, d.2, d.3 データの流れ
- f.1 ビジー信号
- f.2 インクリメント信号
- f.3 デクリメント信号
- f.4 一致信号
- f.5 エンブティ信号

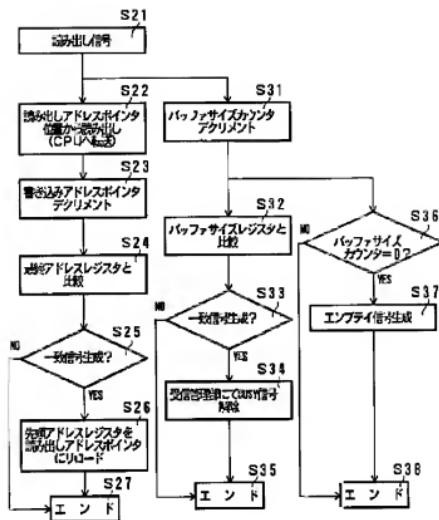
【図1】



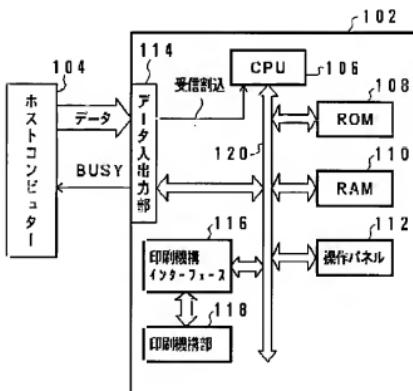
【図2】



【図3】



【図5】



【図4】

